

*REMARKS/ARGUMENTS*

In response to the Office Action mailed August 26, 2005, Applicant amends his application and requests reconsideration. In this Amendment, non-elected 5-8 have been cancelled leaving claims 1-4 pending. Only claims 1 and 2 have been examined.

Of the examined claims, claim 1 is the sole pending independent claim. Therefore, by definition, that claim is a generic claim and, upon its allowance, claims 3 and 4 must be rejoined to the prosecution and allowed.

The invention concerns an integrated circuit, particularly a monolithic microwave integrated circuit that provides regulation of the output power of the circuit so that an active element of the circuit does not breakdown when a relatively high driving signal is applied. That result is achieved by controlling the output power produced by the active element through the connection of a diode section in series between the output electrode, i.e., the third electrode, of the active element and a high-frequency signal output terminal of the semiconductor integrated circuit device. The diode section can take many forms as described in the patent application, for example, with respect to embodiments 1-4 that pertain, generally, to the elected species.

In the first described embodiment, the diode section includes a single unbiased diode connected between the output terminal of the active element, a field effect transistor in the illustrated embodiments, and the output terminal of the device. The polarity of that diode is not important. In the second embodiment, the diode section includes a pair of diodes connected in parallel to each other and in inverse polarity. In the third embodiment, the diode section includes a plurality of diodes connected in like-polarity series. In the fourth embodiment, a single diode is provided as the diode section and a DC bias is applied to that diode in order to control the driving level of the active element at which the loop gain of the circuit reaches an equilibrium state.

Pursuant to a species election requirement and an election, only claims 1 and 2 were examined. Both claims 1 and 2 were commonly rejected over each of two combinations of publications. Both rejections are respectfully traversed.

Claims 1 and 2 were rejected as unpatentable over Shiga (U.S. Patent 5,309,119) in view of Yeh (Published U.S. Patent Application 2004/0095198).

While a lengthy discussion could be provided concerning this rejection, it is sufficient to point out that that Yeh is not prior art to the present patent application and, therefore, the rejection must be withdrawn. The effective date of Yeh is its U.S. filing date, namely March 4, 2003. While the present patent application was filed in the United States on January 23, 2004, upon perfecting the priority claim to JP 2003-014645, the effective filing date of the present patent application is January 23, 2003, before the effective date of Yeh. In order to perfect that priority claim pursuant to 37 CFR 1.55(a), enclosed is a certified English language translation of the priority patent application. The translation clearly shows the support for claims 1-4, as required by 35 USC 112, in the priority patent application, giving the present patent application an effective date of January 23, 2003. Accordingly, the first rejection of claims 1 and 2 must be withdrawn because Yeh is not prior art.

Claims 1 and 2 were also rejected as unpatentable over Shiga in view of Higashiyama et al. (U.S. Patent 5,225,793, hereinafter Higashiyama). This rejection is respectfully traversed.

Applicant agrees with the Examiner's characterization of the disclosure of Shiga. The Examiner acknowledged that Shiga does not show an element corresponding to the diode section of claims 1 and 2, connected between the third electrode of the active element and the output terminal of the semiconductor device structure illustrated in Figure 2 of Shiga.

For the diode section of claim 1, reliance was placed upon the diode limiter 6 illustrated in Figure 1 of Higashiyama. Applicant acknowledges that the limiter 6 shown in Figure 1 of Higashiyama includes two diodes connected in parallel in inverse polarity. However, that limiter 6, like all such devices limiting the amplitude of an output signal, is connected in parallel between the output terminal of the Higashiyama circuit and ground. The limiter 6 in Figure 1 of Higashiyama is not, like the diode section of the claims, connected between the output terminal of the active element, the amplifier 1 in Figure 1 of Higashiyama, and the output terminal of the Higashiyama circuit.

Higashiyama even describes, in column 2 at lines 59 and 60, that "the limiter circuit 6 [is connected to the amplifier 1] to serve as the output terminal of the voltage-control oscillator (VCO). Moreover, Figure 1 of Higashiyama shows that the limiter 6 is

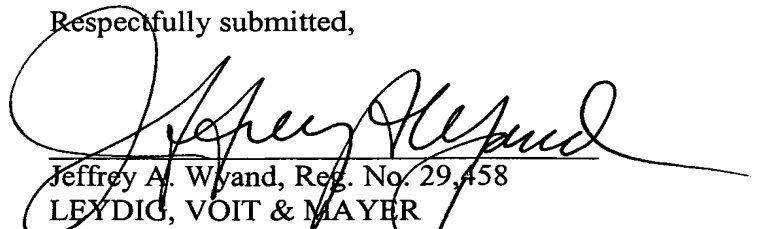
connected between the output terminal of the amplifier 1 and ground. Only the connection to the output terminal of the amplifier 1 could be the output terminal of the circuit of Higashiyama. Thus, assuming the limiter 6 is a "diode section", it is apparent that if the first end of that diode section is connected to the output, i.e., third electrode of the amplifier 1, the second end of the diode section of Higashiyama, which is connected to ground, cannot be considered connected to the signal output terminal of the Higashiyama amplifier. As noted, the connection of the limiter in Higashiyama is a parallel one with respect to the amplifier, so that the circuit illustrated in Higashiyama is different in both structure and function from the circuit of the examined claims. There is no suggestion in Higashiyama or Shiga that the limiter circuit 6 should be connected in series between the output terminal of the amplifying element and the output terminal of the circuit as in the claimed invention. Accordingly, *prima facie* obviousness has not been established and the rejection cannot properly be maintained.

For the foregoing reasons, the rejections of claims 1 and 2 must be withdrawn. Since claim 1 is allowable, claims 3 and 4 must be rejoined to the prosecution and allowed along with claims 1 and 2.

Since no claim has been amended in response to the Office Action, any new rejection based upon newly cited prior art or a different legal ground, cannot properly be a final rejection.

Reconsideration and allowance of claims 1-4 are earnestly solicited.

Respectfully submitted,



Jeffrey A. Wyand, Reg. No. 29,458  
LEYDIG, VOIT & MAYER  
700 Thirteenth Street, N.W., Suite 300  
Washington, DC 20005-3960  
(202) 737-6770 (telephone)  
(202) 737-6776 (facsimile)

Date: February 27, 2006  
JAW:ves